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<b>INFORMATION DISCLOSURE STATEMENT BY APPLICANT</b> <i>( Not for submission under 37 CFR 1.99)</i>	Application Number		10735123	
	Filing Date		2003-12-12	
	First Named Inventor		Igor KELLER	
	Art Unit		2128	
	Examiner Name		Russell Warren Frejd	
	Attorney Docket Number		8195.002.NPUS01	

**U.S.PATENTS**

Examiner Initial*	Cite No	Patent Number	Kind Code <sup>1</sup>	Issue Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear
/RF/	1	7065720	B2	2006-06-20	Croix	

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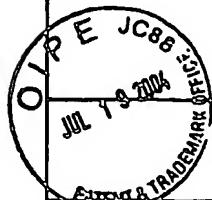
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Form PTO-1449  INFORMATION DISCLOSURE CITATION IN AN APPLICATION  (Use several sheets if necessary)		Docket Number 188122000400	Application Number 10/735,123
		Applicant <i>10/735,123 Igor KELLER et al.</i>	
		Filing Date December 12, 2003	Group Art Unit 2070 2128
		Mailing Date July 15, 2004	



### U.S. PATENT DOCUMENTS

Examiner Initials	Ref. No.	Date	Document No.	Name	Class	Subclass	Filing Date If Appropriate

### FOREIGN PATENT DOCUMENTS

Examiner Initials	Ref. No.	Date	Document No.	Country	Class	Subclass	Translation YES NO

### OTHER DOCUMENTS

(including author, title, Date, Pertinent Pages, Etc.)

Examiner Initials	Ref. No.	Title
RF	1.	R. Arunachalam et al., "TACO: Timing Analysis With COupling", ACM 2000, 4 pgs.
	2.	P. Chen et al., "Miller Factor for Gate-Level Coupling Delay Calculation", IEEE, International Conference on Computer Aided Design, 2000, 7 pgs.
	3.	J. F. Croix et al., "Blade and Razor: Cell and Interconnect Delay Analysis Using Current-Based Models", DAC June 2-6, 2003, Anaheim CA, pp. 386-389.
	4.	F. Dartu et al., "Calculating Worst-Case Gate Delay Due to Dominant Capacitance Coupling", DAC 97, Anaheim CA, 6 pgs, 1997.
	5.	P. D. Gross et al., "Determination of Worst-Case Aggressor Alignment for Delay Calculation", ACM 1998, pgs. 212-219.
	6.	I. Keller et al., "A robust cell-level crosstalk delay change analysis", 8 pgs, NOVEMBER 2004.
	7.	I. Keller et al., "On a robust noise-on-delay cell-level analysis", 7 pgs, DATE UNAVAILABLE.
	8.	A. Odabasioglu et al., "PRIMA: Passive Reduced-Order Interconnect Macromodeling Algorithm", IEEE Transactions on Computer Aided Design of Integrated Circuits and Systems, vol. 17, no.8, Aug. 1998, pgs. 645-654.
	9.	V. Raghavan et al., "AWESpice: A General Tool for the Accurate and Efficient Simulation of Interconnect Problems", 29th ACM/IEEE Design Automation Conference, paper 6.3, 1992, pgs. 87-92.
	10.	K. Shepard, "Design Methodologies for Noise in Digital Integrated Circuits", 35th Design Automation Conference, ACM 1998, 6 pgs.
↓	11.	S. Sirichotiyakul et al., "Driver Modeling and Alignment for Worst-Case Delay Noise", IEEE Trans. on Very Large Scale Integration v. 11, no. 2, April 2003, 6 pgs.
RF	12.	V. Zolotov et al., "Noise Propagation and Failure Criteria for VLSI Designs", IEEE 2002, 8 pgs.

EXAMINER: /Russell Frejd/ DATE CONSIDERED: 07/17/2006

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Examiner Initials	Ref. No.	Date	Document No.	Country	Class	Subclass	Translation YES NO
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